On the Design of Large Receiver and Transmitter Arrays for OE-VLSI Applications

Michael B. Venditti, *Member, IEEE,* and David V. Plant, *Member, IEEE*

***Abstract*—The design environment, design and test flows, and the constraints and challenges of implementing large two-dimensional arrays of receiver and transmitter circuits for optoelectronic-very-large-scale-integration (OE-VLSI) applications is described, and the use of optically and electrically differential architectures is advocated. We show that the incorporation of design-for-testability features and chip-level test methodologies overcome some of the unique challenges of testing OE-VLSI receiver and transmitter circuits. We present design techniques that can be used to improve the switching-noise performance of fully differential OE-VLSI receiver and transmitter circuits. We show that the operational yield of large receiver arrays is maximized through the use of an optically and electrically differential architecture.**

***Index Terms*—Application-specific integrated circuits (ASICs), design for testability, differential optical signaling, driver circuits, mixed analog-digital integrated circuits, optical interconnections, optical receivers, optical transmitters, optoelectronic-VLSI, very-large-scale integration.**

I. Introduction and Motivation

BASED on the recent rapid evolution of electronic and optoelectronic technologies, new opportunities and new constraints have emerged that motivate the analysis of the design and implementation of large, two-dimensional (2-D) arrays of receiver and transmitter circuits for optoelectronic-very-large-scale-integration (OE-VLSI) applications [1]–[3]. An OE-VLSI chip represents a mixed-signal integrated circuit typically using state-of-the-art complementary metal–oxide–semiconductor (CMOS) process technology, in which optical receiver and transmitter circuit arrays are tightly integrated with digital circuitry. The maturation of heterogeneous integration techniques now allows the integration of large 2-D arrays of optoelectronic devices (OEDs), such as vertical-cavity surface-emitting lasers (VCSELs) and photodetectors, to the optical receivers and transmitters on a CMOS chip to form dense arrays of surface-normal optical inputs and outputs (I/Os).

OE-VLSI applications typically have large optical I/O requirements (e.g., in switching applications [4]–[7]), implement complex processing functions operating on wide data busses ([8], [9]) or implement simple processing functions operating on large data sets, but only on a small number of bits at a time (e.g., image processing applications [10], [11]). The digital circuitry is an integral part of an OE-VLSI chip and strongly influences the design environment and the design flow of the optical receivers and transmitters. Integration with digital circuitry, for example, requires the optical receivers and transmitters to operate with low supply voltages and in the presence of substantial amounts of switching noise. Integrating optical I/O with digital circuitry also permits the receiver and transmitter circuits to be treated as replacements or complements to conventional electrical I/O pads or as bridging elements for electrical interconnects. This allows for conventional digital design and test flows to be extended to accommodate optical receivers and transmitters, facilitating the integration of OE-VLSI technology into mainstream applications. This is attractive for the development of new test techniques for OE-VLSI chips, which thus far have been largely ad hoc and nonpervasive with little support provided at the chip level. In many OE-VLSI chips, arrays of OEDs are tested by forward-biasing all of the elements in the array, providing some information on heterogeneous OED integration yield but little information regarding the operability of the receiver or transmitter circuits themselves. Some portions of the receiver and transmitter circuits in [8] could be crudely tested, but the test results were not conclusive. The tests themselves were devised after the circuits had been designed, and the lack of support at the chip level for performing the test made testing a laborious and time-consuming effort. The use of conventional design and test flows in OE-VLSI chip design presents an opportunity for significant advancement in the area of testing.

The analogy of OE-VLSI receivers and transmitters as optical replacements for conventional electrical I/O pads is an ideal starting point for the discussion of OE-VLSI architectures. In high-speed on-chip and off-ship signaling applications, differential signaling formats such as current mode logic (CML), low voltage differential signaling (LVDS), and high-speed transceiver logic (HSTL) are commonplace. The use of a differential architecture for mixed-signal technologies to combat the effects of switching noise and to enhance signal integrity at high data rates has been widely accepted both in industry and in academia for many years. A fully differential (optical and electrical) architecture was identified as a superior architecture for fiber-based and free-space optical interconnects more than a decade ago [12]–[14]. For these reasons, the adoption of an optically and electrically differential architecture in OE-VLSI applications might seem natural. In terms of electrical architectures, however, this has largely not been the case. To the authors' knowledge, only one OE-VLSI chip employing a

Manuscript received January 7, 2003; revised August 27, 2003. This work was supported in part by BAE Systems under a contract via the DARPA/ARL VLSI-Photonics program (DAAL01-98-C-0074, the Natural Sciences and Engineering Research Council (NSERC), the Canadian Microelectronics Corporation (CMC), and the Canadian Institute for Photonic Innovation (CIPI).

M. B. Venditti was with the Department of Electrical and Computer Engineering, McGill University, Montreal, QC, H3A 2A7. He is now with PMC-Sierra, Inc., Ville Mont-Royal, QC, H3R 3L5, Canada, (e-mail: michael_venditti @pmc-sierra.com).

D. V. Plant is with the Department of Electrical and Computer Engineering, McGill University, Montreal, QC, H3A 2A7, Canada (e-mail: plant@photonics.ece.mcgill.ca).

Digital Object Identifier 10.1109/JLT.2003.822234

differential optical and electrical architecture has been reported to date [8]. Some OE-VLSI chips utilizing a differential optical signaling architecture have been reported ([4]–[6], [15], [16]), but the underlying electrical architecture of the receiver and transmitter circuits on these chips were single-ended. The use of differential optical signaling for these chips was intended primarily to address the weak optical signal contrast available from quantum-confined Stark effect (QCSE) modulator-based transmitters. In [16], for example, a totem pole QCSE modulator structure was used to transmit differential optical data from an electrically single-ended transmitter circuit (a CMOS inverter) and achieve a contrast ratio of 2:1. The receiver was based on an electrically single-ended transimpedance amplifier and used a similar totem pole QCSE detector structure to decode the differential optical input.

There are two principal differences between the design of receivers and transmitters for OE-VLSI applications and for others such as telecommunicatiosn and data communications applications. First, the pitch of the OEDs in the OED array limits the physical space available to implement a receiver and transmitter circuit in an OE-VLSI application. OED pitches have become quasistandardized to a 125-μm grid [8], [17]. This permits at most a 125×125-μm are (for an optically single-ended design) or a 125×250-μm are (for an optically differential design) to implement the receiver and transmitter circuit. Second, there is the concern of aggregate power dissipation in large arrays. In [8], for example, the maximum power dissipation of a receiver circuit was approximately 9.5 mW. If all receivers were operated simultaneously, the aggregate power dissipation of the 540-element array would be more than 5 W.

These differences place severe constraints on the design of a receiver and transmitter circuit for OE-VLSI applications. The type of circuit elements that can be used for an OE-VLSI receiver and transmitter is limited. The ability to use on-chip passive circuit elements, such as resistors, capacitors, or spiral inductors, is limited or impossible due to the size of the elements. Active devices often serve as replacements for passive circuit elements. For example, the use of metal–oxide–semiconductor field-effect transistor (MOSFET) devices as resistive feedback elements in receiver preamplifiers is well established. MOSFET devices have also been used to implement active inductor loads in receiver applications [18], [19] and are also commonly used to implement power supply or bias voltage decoupling capacitors.

Physical space limitations can also limit the circuit complexity that can be realized for an OE-VLSI receiver and transmitter. Serialization and deserialization operations and data encoding schemes, such as 8-b/10-b coding, commonly found in telecommunications and data communications applications, are avoided to allow the implementation of a simplified dc-coupled receiver [4]. Other circuit features common to non-OE-VLSI applications can require significantly more area to implement than is available. For example, a receiver with automatic gain control can occupy an area of more than 650×1200 μm [20]. In [21], a clock and data recovery circuit occupied more than 600×700 μm. These constraints are more severe for the receiver and, consequently, it must employ a simple design [17], [22], [23].

Conversely, OE-VLSI receiver and transmitter circuit design has some unique challenges as compared with their telecommunications or data communications counterparts. The most significant challenge arises from the use of an optical system to perform a chip-to-chip or intra-chip interconnection of dense 2-D arrays of optical signals. Although such large-scale optical systems have been successfully constructed, they introduce spatial losses that are significantly nonuniform across the array. For example, a clustered microoptical system designed to relay 512 optical beams arranged as 32 4×4 clusters of beams was found to have power transmission variations from the mean of $\pm 35\%$ within a typical cluster [24]. Another optical system for an 8×8 array of optical beams based on a fiber image guide with 10-μm diameter fibers and 1.4-μm claddings was found to exhibit power transmission variations from the mean between ± 10 and $\pm 35\%$, depending on the input spot radius [25]. This degree of power transmission nonuniformity can cause significant operational problems for an array of electrically single-ended receiver circuits that are commonly biased and controlled, as all such receivers have the same decision threshold. In an optically differential transmission scheme with an electrically differential receiver, the problem of power transmission nonuniformity in the optical system is limited to the two differential inputs to any given receiver. For this reason, the use of an optically and electrically differential architecture is particularly attractive for OE-VLSI applications.

The organization of this paper is as follows. Section II describes design-for-testability (DFT) techniques and testing for OE-VLSI receivers and transmitters. In this section, we describe the implementation of circuit-level DFT features, a formal approach to fault sensitization and detection, and the integration of receiver and transmitter test methodologies compatible with conventional digital VLSI chips. Section III presents a discussion of switching noise in receiver and transmitter arrays, outlining the benefits offered by a fully differential architecture and addressing some receiver and transmitter design considerations to improve switching-noise performance. Section IV describes the effects of switching noise and variations in incident optical power on the operational yield of commonly biased and controlled groups of receiver and transmitter circuits. Section V is the conclusion.

II. Design for Testability

The incorporation of DFT features, such as serial scan chains (SSCs) and level-sensitive scan design, are commonplace in digital system design [26], [27]. Testability concepts have been extended to analog and mixed-signal circuitry ([28], [29]) and to small transmitter arrays ([30]), but these approaches are not appropriate for OE-VLSI applications due to the scale of the receiver and transmitter arrays, where circuits can number in the hundreds or thousands. This section will discuss the testing of large arrays of receiver and transmitter circuits in OE-VLSI applications and the means of incorporating circuit-level testing with chip-level techniques commonly employed with digital circuitry.

OE-VLSI receivers and transmitters are unique given that the receiver input and transmitter output are optical and that the OEDs, via a heterogeneous integration technique such as

flip-chip bonding, are an integral part of the circuit topology. The task of testing such circuits is complicated because conventional test equipment for mixed-signal and digital VLSI chips do not have optical I/O capabilities. Furthermore, heterogeneous OED integration introduces cost and yield issues beyond that normally associated with digital VLSI chips. The heterogeneous integration process may, for example, detrimentally affect the operation of the OEDs, resulting in dead receivers, dead transmitters, or dead digital circuitry and rendering part or all of a chip nonfunctional. in addition, some of the electrical connections between the OED arrays and the VLSI chip (e.g., the flip-chip bump bonds in a flip-chip bonding heterogeneous integration process) may be poor or completely open-circuited after the heterogeneous integration process. For reasons such as these, it is desirable to perform circuit testing both before and after heterogeneous OED integration.

The following subsections describe test features at the circuit level of the receiver or transmitter that can be easily incorporated. These test features allow for electrical-only tests that do not rely on the presence or absence of OEDs in the circuit topology and can assist in the detection of functional faults within the constraint of using electrical test equipment without optical I/O capability. The successful post-integration testing of the OEDs and OED connections would require large-scale optical I/Os to be available with test equipment and, thus, cannot be addressed using the techniques described in this section. Test methodologies that integrate receiver and transmitter testing with conventional digital test methodologies at the chip level are also discussed. It will be shown that the implementation of these test techniques are facilitated by differential architectures.

A. DFT Implementation

To facilitate the basic testing of receivers and transmitters, circuit elements can be added in parallel with the normal OED locations to mimic their electrical behavior. This is illustrated in Fig. 1 (MT transistors) for optically and electrically differential (a) preamplifier and (b) transmitter circuits [8]. When enabled, these transistors allow the injection of current into either of the input arms of the preamplifier to mimic a photocurrent input and allow paths for current conduction to be enabled for the transmitter. When disabled in normal operation, the additional parasitic capacitance of the DFT circuit elements has only a minor performance impact as they are small (tens of femtofarads) with respect to the junction capacitance of the OEDs (hundreds of femtofarads).

Although the incorporation of these additional circuit elements facilitates receiver and transmitter testing, they are, in isolation, limited to performing circuit-level or group-level testing. For the receiver in [8], only basic pass/fail testing could be performed on individual circuits; for the transmitter, only qualitative pass/fail testing could be performed on groups of circuits simultaneously through supply current monitoring. In order for OE-VLSI technology to be commercialized, it is necessary to proceed beyond the addition of simple DFT features on a per-circuit basis. A formal sensitization and detection process and the incorporation of testing features at higher levels of the chip design are required.

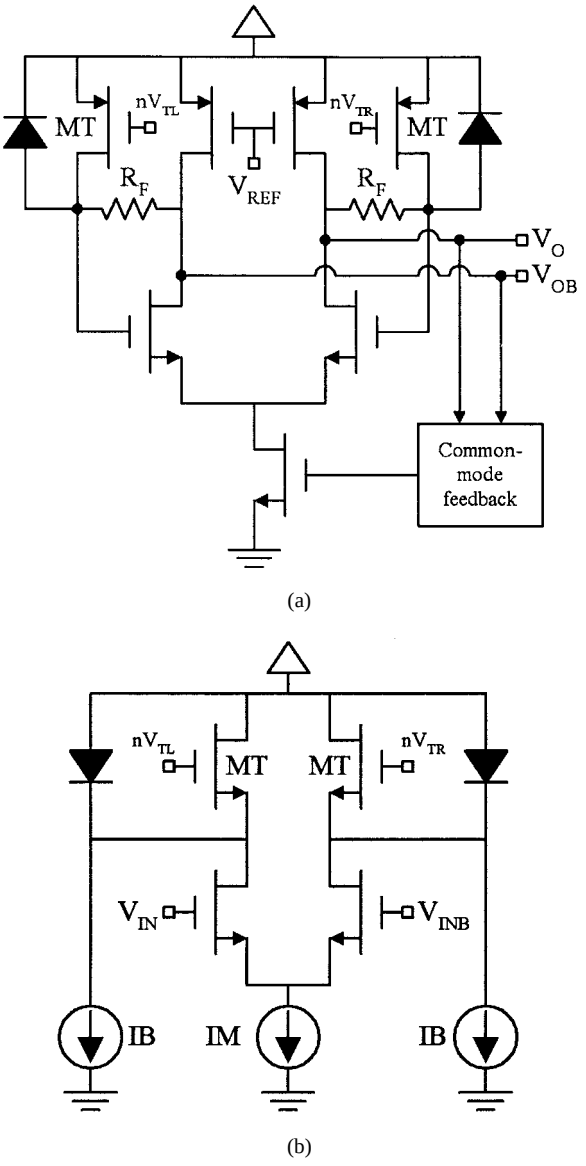

Fig. 1. Incorporation of DFT features in optically and electrically differential (a) receivers and (b) transmitters [8]. Additional circuit elements (MT transistors), controlled by inputs nV_{TL} and nV_{TR}, are added in parallel with the normal locations of the OEDs (shown as diodes) to mimic their electrical behavior.

B. Obtaining Test Results

To test receiver and transmitter circuits and to maintain compatibility with conventional digital VLSI test techniques, a digital result from the circuit under test is required. This can be accomplished by using a comparator to compare various node voltages in the circuit under test to each other or by monitoring the outputs of circuit stages that produce CMOS logic voltage levels.

The comparator approach is facilitated through the use of an electrically differential architecture, where complementary circuit nodes with symmetric behavior abound and can be easily compared against one another. In electrically single-ended architectures, internal circuit nodes would need to be compared with reference voltages generated from on-chip voltage reference or replica circuits. The comparator circuitry can be designed such that it dissipates no power and has minimal (tens

of femtofarads) capacitive loading effects during normal operation. The only significant penalty is an increase in circuit layout area, which is discussed further in Section II-D.

C. Fault Sensitization and Detection

Typical CMOS manufacturing faults include open-circuit and bridging faults [31]. Setting the controllable inputs to the circuit under test to establish an expected fault-free circuit state (referred to as a test vector) sensitizes faults in the receiver and transmitter. Assuming a single-fault model, the test vector sensitizes all faults that could lead to a state other than the fault-free state. Once the test vector is applied, the circuit state is checked. If the circuit state is not equal to the fault-free state, a fault is detected.

As an example, consider the optically and electrically differential transmitter circuit shown in Fig. 2. A number of possible faults are indicated in brackets, with $(\,)$'s representing open-circuit faults and $\langle\,\rangle$'s representing bridging faults. With the $\mathrm{nV_{TL}}$ and $\mathrm{nV_{TR}}$ inputs set high to enable the test structures, many of the indicated faults can be sensitized using the following test vector: set input $\mathrm{V_{IN}}$ high and input $\mathrm{nV_{IN}}$ low to steer the modulation current (IM) to the left-hand side of the circuit; set the left-hand side bias current (IBL) to a nominal magnitude and set the right-hand side bias current (IBR) and IM to $2 \cdot \mathrm{IBL}$ and $4 \cdot \mathrm{IBL}$, respectively. For this test vector, the fault-free circuit state corresponds to node voltage $\mathrm{V_L}$ less than node voltage $\mathrm{V_R}$. If $\mathrm{V_L} > \mathrm{V_R}$ results from the application of the test vector, one of many possible faults has been detected. This includes faults (2, 4) and $\langle 4, 6\rangle$ that result in $\mathrm{V_R}$ being pulled toward ground, fault $\langle 1\rangle$ that results in $\mathrm{V_L}$ being pulled toward the supply voltage, and faults (5, 7, 9, 10) that prevent IM from being steered to the left-hand side of the circuit.

D. Test Overhead

To quantify the circuit layout overhead of incorporating comparator circuit(s) to generate digital test results for receiver and transmitter circuits, a test chip in 0.35-μm CMOS was fabricated. The test chip was designed to ensure that open-circuit and bridging faults could be detected reliably across all process corners using the methods described thus far in this section. Faults were manually inserted in multiple replicas of the circuit, and detection of these faults was verified successfully in the fabricated chip. A fully differential receiver was implemented on this chip and included four comparator circuits—one each for the preamplifier and postamplifier, and one each for their corresponding common-mode feedback (CMFB) circuits. The complete receiver occupied 76×61.1 μm, with the test circuitry consuming approximately 42% of the total area. This large overhead is commensurate with the number of independently testable circuit stages. The layout of a fully differential single-stage transmitter circuit on the same test chip occupied 37.9×58.4 μm, with test circuitry corresponding to approximately 22% of the total area.

In digital circuit testing, it is estimated that a 1–3% area overhead for circuit structures dedicated to testing is sufficient to implement sophisticated built-in test schemes [27]. For receiver and transmitter circuit testing, per-stage area overheads of more than 20% are very large by comparison. It is possible to reduce

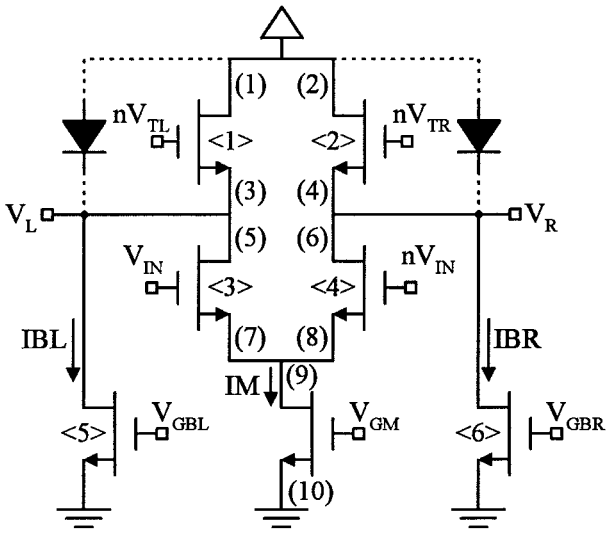

Fig. 2. Fault sensitization and detection example for an optically and electrically differential transmitter. $(\,)$'s indicate possible open-circuit faults. $\langle\,\rangle$'s indicate possible bridging faults. Dashed lines indicate the normal location of the VCSELs when present.

the layout overhead of testing multistage circuits such as receivers by reducing the number of comparators used. For example, it is possible to use a single comparator or the digital receiver output to obtain test results for cascaded circuit stages that follow the signal path of the receiver, such as the preamplifier and post-amplifier; when testing the preamplifier, the outputs of the post-amplifier could be compared to detect faults. For circuit stages that do not follow the signal path of a multistage circuit, such as CMFB circuits, analog multiplexers can be used to select the inputs provided to a single comparator. Using these approaches, the receiver layout overhead experienced on the test chip could be reduced to 21% from 42%. If the digital output of the receiver rather than a comparator were used to generate digital test results for circuit stages that follow the signal path, the receiver layout overhead could be reduced to approximately 10%. Simulations performed on the test-chip receiver design verified that all preamplifier faults that could be detected using a comparator to compare the outputs of the preamplifier could still be detected by using a comparator to compare the outputs of the post-amplifier instead. This suggests that fault coverage will not be compromised using these overhead-reduction techniques.

E. Chip-Level Implementation

Conventional testing methodologies in digital VLSI at the chip level, such as the use of SSCs, can also be used for OE-VLSI chips to integrate receiver and transmitter testing with conventional digital testing. SSCs can be used at the interface between a receiver array and a combinational digital circuit and between a combinational digital circuit and a transmitter array. Fig. 3 illustrates an example of receiver-side SSC cells [32] that can be linked to other cells to form SSCs. The corresponding transmitter-side SSC cell is similar. The SSC cell in Fig. 3(a) can be used to scan in control and test inputs to an array of receivers or to the digital circuit. The D flip-flop (DFF) with a strobe signal for the clock is used as a means to apply the

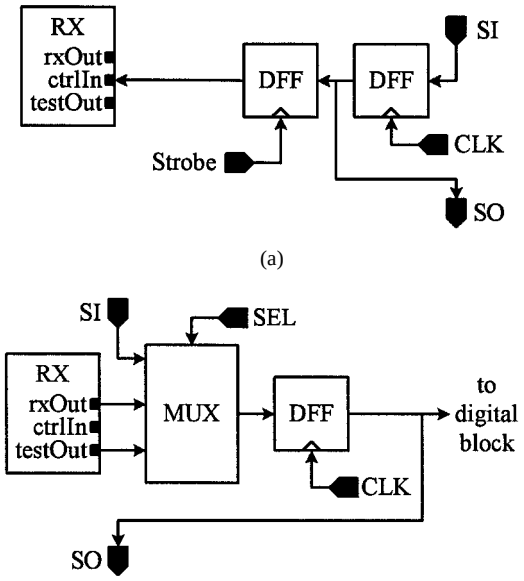

Fig. 3. Receiver-side SSC cells to (a) scan in control and test inputs to the receiver array or to the digital circuit and (b) scan out test responses, receiver outputs, or to provide a pass-through path for normal operation. The scan-out (SO) pin of a cell can be linked to the scan-in (SI) pin of a subsequent cell to form an SSC.

control and test inputs to all of the receivers only after scanning in is complete. The SSC cell in Fig. 3(b) can be used to scan out test responses from the receiver array, the receiver outputs, or to provide a clocked pass-through path from the receiver array to the digital circuit in normal operation.

III. Switching Noise

Telecommunications and data communications receivers are often operated in isolation on a given chip and designed for noise-limited (i.e., thermal, shot, or flicker noise) sensitivity. In OE-VLSI applications, receivers and transmitters are implemented in large arrays using a state-of-the-art CMOS process technology and must operate with low supply voltages and in the presence of substantial amounts of switching noise from the surrounding digital circuitry. Consequently, the performance of OE-VLSI receivers and transmitters are limited by the effects of switching noise and by random dc offsets arising from transistor mismatch [7], [22], [33]. This implies that an electrically differential architecture, due to the inherent common-mode rejection capability that it offers, can be used advantageously in OE-VLSI applications to combat the detrimental effects of switching noise. The surrounding digital circuitry and the receiver and transmitter arrays generate switching noise in an OE-VLSI environment, appearing as a voltage signal superimposed on the power supply rails. Switching noise can couple into neighboring victim circuits directly through the power supply networks and through the substrate and indirectly through capacitive coupling of independent power supply networks and signal paths. When the victim circuit is a transmitter, switching noise can couple into the optical output and be transmitted optically to the input of a receiver on another chip. In all cases, switching noise degrades the performance of the victim circuit and/or requires additional power to compensate for it. In [33], the switching noise generated through the parallel operation of a 50-element single-ended receiver array was shown to result in degraded receiver sensitivity (a 3-dB power penalty) over that of a receiver operating in isolation. In [17], switching noise was found to affect the performance of the single-ended transmitter circuits. As more proximally located transmitter circuits were operated, the effects of switching noise resulted in a deteriorated eye diagram.

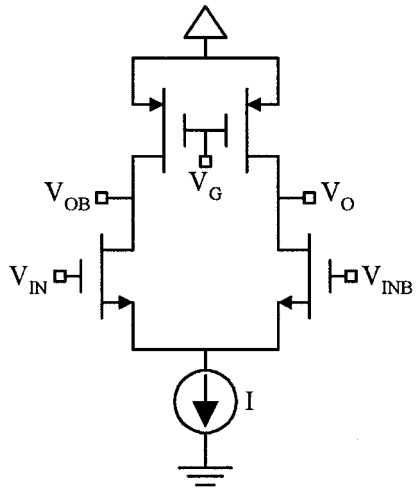

Fig. 4. Representative schematic of a fully differential amplifier stage.

In the following subsections, the switching-noise performance of receiver and transmitter circuits are discussed qualitatively, along with various design techniques that a designer may consider to improve switching-noise performance.

A. Receivers

The need to interface with digital CMOS circuitry demands that later receiver circuit stages operate nonlinearly and produce large voltage signals approaching the voltage supply rails. In this respect, they have switching-noise generation and immunity characteristics similar to digital CMOS circuitry, in which noise is generated during logic-state transitions. In [8], [17], and [34], a Schmitt trigger was used to improve the switching-noise immunity of a receiver by introducing hysteresis in the transfer characteristic (TC) of the decision stage. The drawback to this approach is that only these later receiver stages benefit from it. Signal contamination in earlier circuit stages can still result in an erroneous input to the Schmitt trigger.

In contrast, the initial circuit stages of a receiver such as the preamplifier generally work as linear amplifiers operating on small voltage signals. It is these circuit stages that are most susceptible to the effects of switching noise. Electrically single-ended receivers have less immunity to switching noise than receivers with an electrically differential architecture because they do not have any common-mode rejection capability. From a switching-noise perspective, the optimal architecture for a receiver amplifier stage is a fully differential one, such as that shown in Fig. 4, which has symmetry in the voltage waveforms at complementary circuit nodes. This causes switching noise to be coupled symmetrically into both the V_O and V_{OB} outputs and to appear as a common-mode signal at the inputs to the next amplifier stage, where it can be rejected.

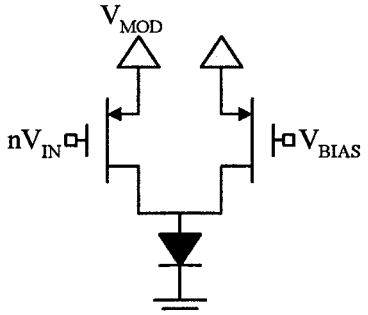

Fig. 5. Transmitter based on current switching [30]. The entire modulation current (whose magnitude is set by V_{MOD}) is switched every time the input undergoes a transition.

B. Transmitters

In the current switching transmitter shown in Fig. 5 [30], the entire modulation current, whose magnitude is set by the voltage V_{MOD}, is switched every time the transmitter undergoes a logic state transition, causing a large amount of switching noise to be generated. This is inappropriate for large arrays of transmitter circuits. In OE-VLSI applications, a transmitter design based on current steering, as illustrated in Fig. 6, is required. In a current steering transmitter, the modulation current (IM) is steered (a) between the VCSEL and a dummy load in an optically single-ended configuration or (b) between two VCSELs in an optically differential configuration. For the optically single-ended configuration shown in Fig. 6(a), there is an asymmetry in the electrical properties of the two paths in which the modulation current can flow. This causes the drain-source voltage across the IM tail current source to be different in each logic state, resulting in a logic-state dependence in the drawn supply current. For the optically differential configuration shown in Fig. 6(b), where the dummy load of Fig. 6(a) is replaced by another VCSEL, and each is provided its own bias current (IB), the asymmetry in the electrical properties of the two paths in which the modulation current can flow is largely eliminated.

For both the optically single-ended and differential transmitters of Fig. 6, switching noise is generated during input transitions due to the asymmetry of the current waveforms through steering transistors M1L and M1R. The transmitter inputs (V_{IN} and nV_{IN}), which are rail-to-rail CMOS logic signals, control the operation of M1L and M1R, causing them to conduct current or to be in cutoff. The portion of the input swing of $V_{IN}(V_{INB})$ from a low-to-high voltage transition for which the gate-source voltage of M1L (M1R) is less than its threshold voltage is wasted, as it does not significantly change the conductivity of M1L (M1R). During this period, the conductivity of M1R (M1L) is being reduced in conjunction with a high-to-low voltage transition of $V_{INB}(V_{IN})$. This results in asymmetric M1L and M1R current waveforms during input transitions, which causes the voltage at their common-source node [V_X in Fig. 6(b)] to fall and rise as the capacitance at that node is discharged and recharged by the nonstatic current provided by the IM tail current source.

Improved symmetry of the M1L and M1R currents could be achieved through the use of an input conditioning circuit that raises the voltage level of $V_{IN}(V_{INB})$ in the logic low- (high-) state in a manner that tracks the magnitude of the modulation current, eliminating the wasted portion of the input swings during input transitions. Fig. 7 schematically illustrates the im-

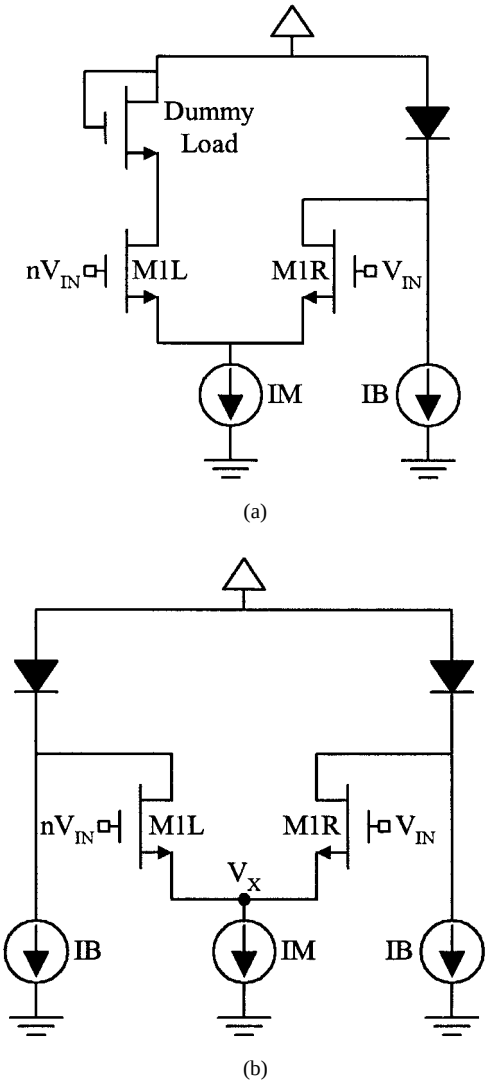

Fig. 6. Transmitters based on current steering. (a) Optically single-ended design. (b) Optically differential design. The modulation current (IM) is always drawn from the supply, being steered through transistor M1L or transistor M1R, depending on the logic state of the complementary V_{IN} and nV_{IN} inputs.

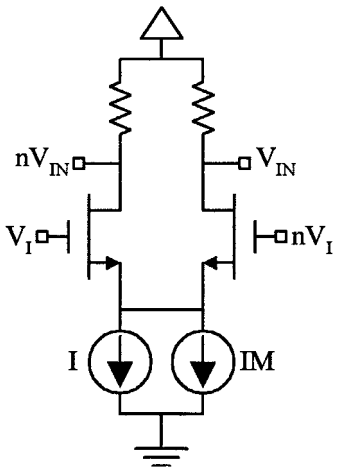

Fig. 7. Representative input conditioning stage used to improve the symmetry of the steered currents in a current steering transmitter [35]. The conditioned low-state voltage for the transmitter inputs is determined by the characteristics of the resistors and the modulation current magnitude (IM). As IM increases, the logic low- (high-) state voltage for $V_{IN}(nV_{IN})$ decreases, and vice versa.

plementation of the conditioning stage from [35]. The outputs of the stage serve as the inputs to the VCSEL-driving stage [such as the circuit of Fig. 6(b), for example]. The conditioned logic low- (high-) state voltage level for $V_{IN}(nV_{IN})$ is dependent on the characteristics of the load resistors and the magnitude of the modulation current. As the modulation current increases, the low- (high-) state voltage at $V_{IN}(nV_{IN})$ needed by M1L (M1R) decreases along with the node voltage V_X because M1R (M1L) requires a larger gate-source voltage.

IV. Receiver Operational Yield

In OE-VLSI ASICs that employ large arrays of receivers and transmitters, there is a practical need to bias and control circuits in groups from a packaging perspective to conserve the required number of external I/O pins. It is also necessary to ensure that circuits have sufficient operational flexibility to overcome any problems arising from, for example, silicon or photodetector process variations or an average input power that varies across the receiver array. Insufficient operational flexibility for a group of receivers can result in the inability to simultaneously operate the entire group of circuits successfully. Receivers in a receiver group may be functional when operated individually, but some may experience problems such as duty cycle distortion or stuck-at 1/0 behavior when many of them are operated simultaneously. In this section, we investigate the effects of variations in incident optical power and the effects of switching noise on the operational yield of receiver common bias and control groups (CBCGs). We show that the operational yield of optically and electrically differential receiver CBCGs is inherently superior to that of optically single-ended ones.

Operational yield is a metric that characterizes the ability of an entire group of circuits to be operated successfully. It is defined as the percentage of circuits in a CBCG that can be simultaneously operated at a desired data rate with a desired bit-error rate (BER). It is possible for individual circuits within a CBCG to meet these performance criteria when operated individually and yet fail to do so when other circuits in the group are also operated. Receiver operational yield is reduced by dynamic operating problems such as switching noise, which degrades receiver sensitivity and BER and worsens as the CBCG size and the data rate increase. It is also compromised by static operating problems such as the inability to set one or more common bias or control parameters to simultaneously configure all of the receivers in the group to meet the desired data rate and BER criteria. It will be shown that the effects of switching noise tend to exacerbate the operational yield problems arising from static control issues.

A. Operational Yield Limitations of Single-Ended Receivers

The electrical TC of a single-ended optical receiver relates the output voltage to the input photocurrent. Fig. 8 shows the noninverting TC for the receiver in [17]. The TC transition region is bounded on both sides by ranges of input photocurrents that correspond to logic 0 and logic 1 receiver outputs. At the center of the transition region, midway between the power and ground rails, is the optimal average input photocurrent (I_{OPT}). For any set of configurable bias and control parameters, there is a corresponding TC and transition region location. Thus, the location of I_{OPT} is bias and control dependent.

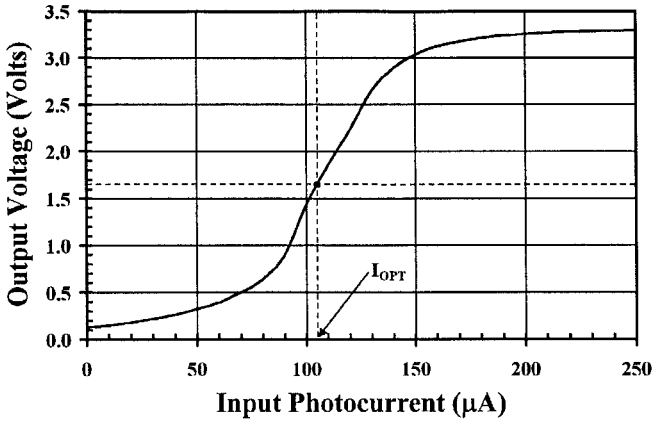

Fig. 8. Representative single-ended receiver TC [17] relating its output voltage to its input photocurrent. The transition region is bounded by input photocurrent ranges corresponding to logic low and logic high outputs. The optimal operating point (I_{OPT}) is at the center of the transition region and its location is bias and control dependent.

From a qualitative operational perspective, the extent to which the average input photocurrent (I_{AVG}) deviates from I_{OPT} determines whether the receiver is operating optimally, the degree to which it is operating successfully but imperfectly, or whether it is not operational at all. Also important is the relative magnitude of the input photocurrent swing (Δi_{PH}) to the width of the TC transition region (ΔI_{TC}). Ideally, I_{AVG} is equal to I_{OPT} and Δi_{PH} is much larger than ΔI_{TC}. When this occurs, the input photocurrent corresponding to the logic high and logic low states extend symmetrically beyond either edge of the TC transition region, providing the output voltage signal with a perfect duty cycle and an optimal eye diagram. When I_{AVG} is smaller (larger) than I_{OPT}, the input photocurrent in the logic low (high) state extends farther beyond the left (right) edge of the TC transition region than the input photocurrent in the logic high (low) state extends beyond the right (left) edge. In both cases, the output voltage signal will exhibit duty-cycle distortion and a reduced eye-diagram opening. As I_{AVG} deviates farther from I_{OPT}, the severity of the duty cycle distortion and the eye-diagram degradation worsen. These problems also worsen as Δi_{PH} gets smaller. If I_{AVG} deviates sufficiently from I_{OPT} or Δi_{PH} is not sufficiently large, the receiver may eventually exhibit stuck-at 1/0 behavior, where it remains stuck in the logic high- or low-output state. Switching noise on the power supply is also problematic, as the TC transition region of a single-ended receiver is affected by changes in the supply voltage. This fact has been used explicitly as a means of offset control in single-ended receivers that had an otherwise fixed TC to achieve optimal operation for a given I_{AVG} [36]. Shifts of the TC transition region due to power supply switching noise is manifested as jitter.

Single-ended receivers in a CBCG are all configured to have the same nominal TC and I_{OPT}. For optimal operation, it is necessary to provide each receiver in the CBCG with the same I_{AVG}, and for it to be coincident with I_{OPT}. This is not possible to achieve perfectly for a number of reasons. In practice, individual receiver TCs in a CBCG may have slightly different characteristics due to silicon process variations. The resulting I_{OPT} for the group of receivers is actually a range of currents. In OE-VLSI applications, it is beyond the control of the circuit designer to achieve a uniform I_{AVG} across a receiver CBCG. The

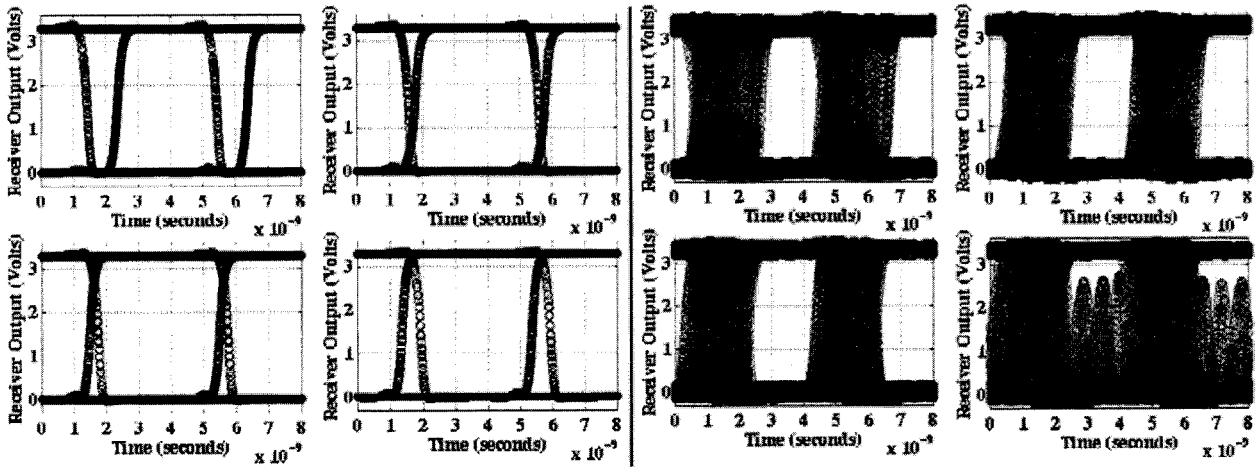

Fig. 9. Four simulated eye diagrams of an eight-element CBCG of optically single-ended receivers [17] at 250 Mb/s. Switching noise was superimposed on the voltage supply and ground rails with amplitudes of (a) 0 mV and (b) 100 mV. The average input photocurrent for each receiver was varied by $\pm 20\%$ across the CBCG. Even without switching noise included, duty-cycle distortion is evident. With switching noise included, the eyes are severely degraded. The eye diagrams for the remaining four receivers were fully closed with switching noise included.

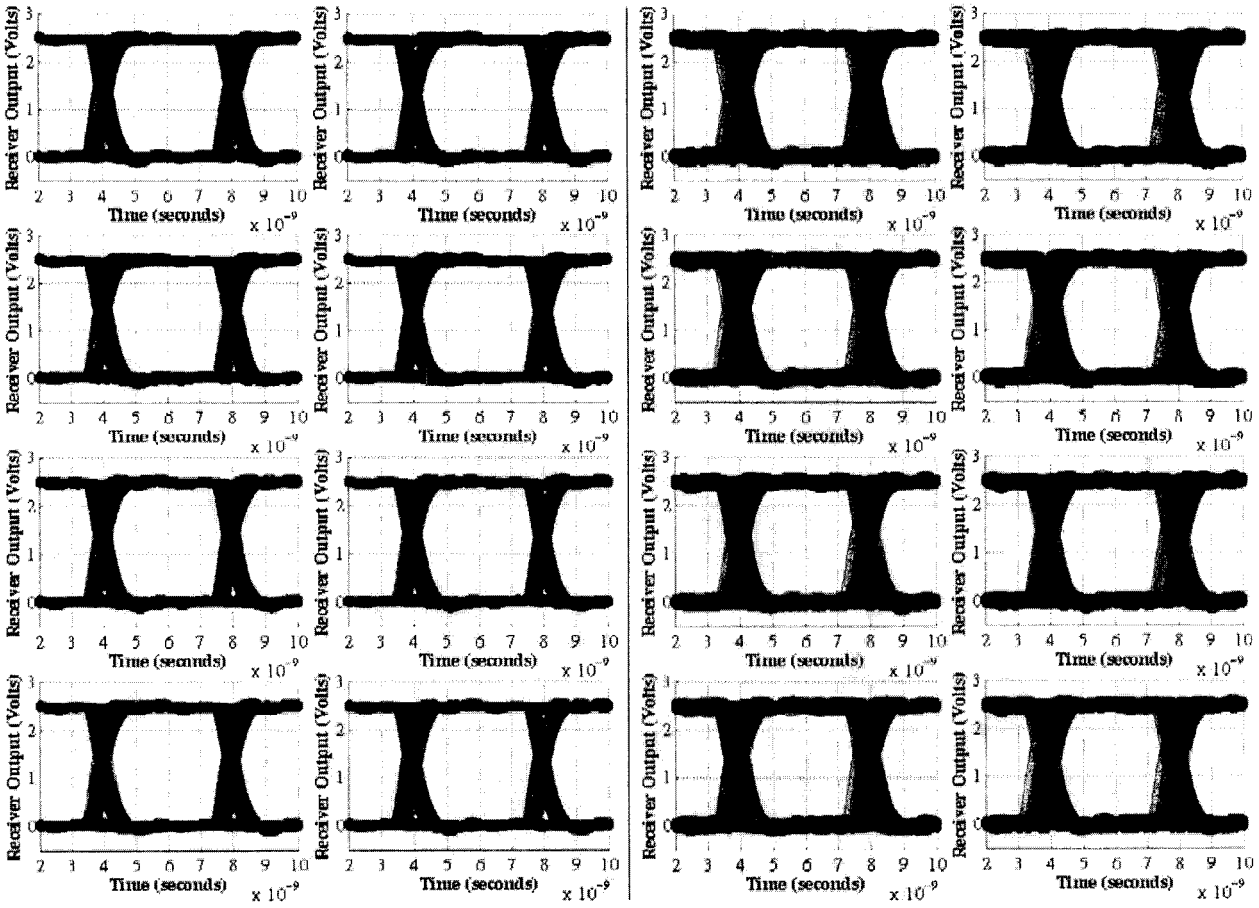

Fig. 10. Simulated eye diagrams of an eight-element CBCG of optically and electrically differential receivers [8] at 250 Mb/s. Switching noise was superimposed on the voltage supply and ground rails with amplitudes of (a) 0 mV and (b) 100 mV. The average input photocurrent for each receiver was varied by $\pm 20\%$ across the CBCG. All eyes are exemplary, even with switching noise included.

degree to which I_{AVG} varies across the receivers in the group is determined by several factors, including the uniformity of the properties of the transmitter circuits and VCSELs that are used to generate the optical signals incident on the group of receivers, the uniformity of the properties of the photodetectors attached to the group of receivers, and the throughput uniformity of the optical system that is used to deliver the transmitted optical signals to the group of receivers. As described in Section I, large-scale optical imaging systems generally suffer from poor power throughput uniformity.

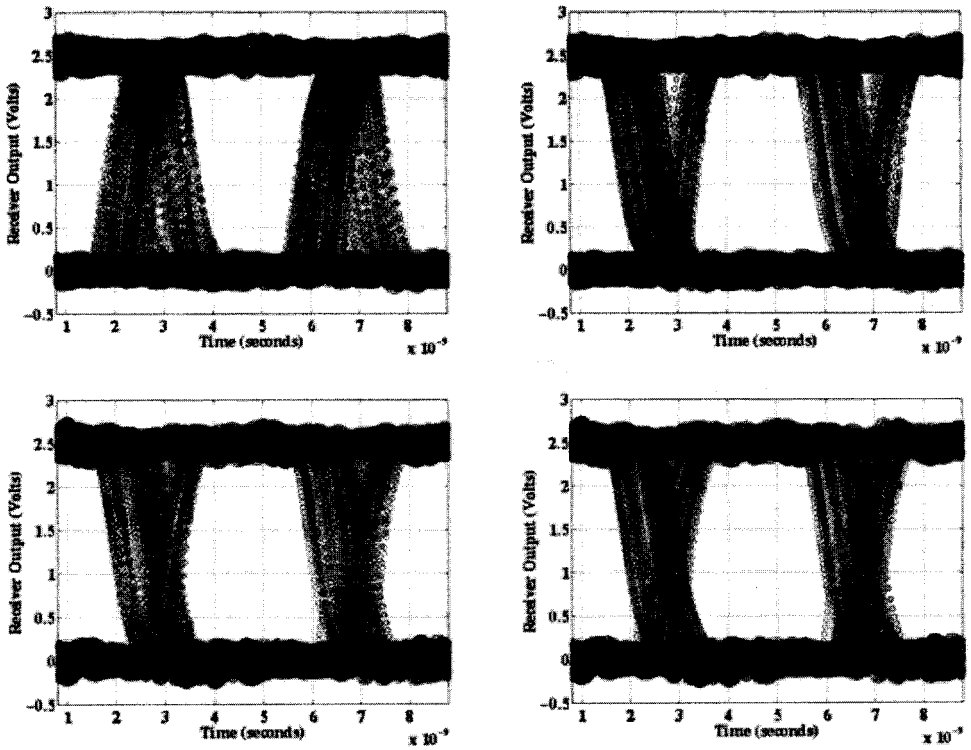

Fig. 11. Simulated eye diagrams of an optically and electrically differential receiver [8] at 250 Mb/s, illustrating the effects of nonuniformities in I_{AVG} and Δi_{PH} for its differential inputs. Switching noise was superimposed on the voltage supply and ground rails with an amplitude of 100 mV. The nominal I_{AVG} is 55 μA and Δi_{PH} is 50 μA. (a) I_{AVG} reduced by 20% for the inverting input. (b) I_{AVG} reduced by 20% for the noninverting input. (c) Δi_{PH} reduced by 20% for the inverting input. (d) Δi_{PH} reduced by 20% for the noninverting input.

The need to provide all the receivers in a CBCG with a uniform I_{AVG} to achieve optimal operation is problematic. In practice, the configurable CBCG parameters must be tweaked to obtain optimal operation for as many receivers as possible for a given optical power swing. Ultimately, if the variation in I_{AVG} across the receiver CBCG is too large to be compensated by parameter tweaking or by increasing the optical power swing, duty-cycle distortion or stuck-at 1/0 behavior will result for one or more receivers, causing the operational yield of the CBCG to decrease. This was experienced in [17], where the operational yield was found to be poor at any data rate ($\leq 25\%$), worsening by approximately 4% per decade with an increasing data rate.

B. Solutions Using Optically and Electrically Differential Architectures

Given these problems, it is necessary to implement receiver designs that are immune to problems that affect operational yield. We contend that the use of optically and electrically differential receiver architectures is the best approach to obtaining maximum operational yield in OE-VLSI applications. As discussed in Section IV, a fully differential electrical architecture provides immunity to the effects of switching noise. It also avoids the fixed decision threshold problems in optically single-ended receivers but without the need to implement area-intensive automatic offset control circuitry; the decision threshold can be derived directly from the optical input signals without regard to neighboring receivers. This essentially shifts the scope of optical-power-level uniformity requirements for high operational yield from the optical inputs of the entire CBCG (the single-ended case) to the complimentary optical inputs of a single receiver (the differential case).

To demonstrate the operational yield superiority of a fully differential receiver design [8] over that of a single-ended receiver design [17], a simulation-based test bed was developed using SPICE. Eight-element CBCGs were constructed for each design, following their transistor-level implementations. The full resistive and capacitive parasitics of the on-chip power distribution network, the inductance of the bonding wires for off-chip power connections, and the resistive and capacitive parasitics of the electrical interconnects driven by the receiver outputs were all included in the model. A $2^9 - 1$-b length pseudorandom bit sequence (PRBS) was generated using a linear feedback shift register (LFSR) implemented in a Matlab script, generating a piecewise linear (PWL) input data file. This file was used for the input data of a PWL voltage source in the simulation. The input data patterns to all of the receivers were derived from the PRBS output, and I_{AVG} and Δi_{PH} were set for each receiver using voltage-controlled current sources. I_{AVG} for the receivers in the CBCG was varied between 45 and 65 μA, representing approximately a $\pm 20\%$ variation from the mean. Δi_{PH} was kept constant at 50 μA for each receiver. For the single-ended design, optimal biasing and control settings were determined for $I_{AVG} = 55$ μA and Δi_{PH} equal to 50 μA, and these parameters were used for the entire CBCG for subsequent simulations. Power-supply switching noise was modeled by superimposing sinusoidal voltage waveforms on the power supply and ground rails. The amplitudes of these noise sources were varied to model different magnitudes of switching noise from surrounding circuitry.

Simulations were performed at 250 Mb/s—the targeted operating data rates for the differential design. It should be noted that the single-ended receiver was functional experimentally at data rates as high as 400 Mb/s. Simulation results were exported and post-processed using Matlab to generate centered eye diagrams, which are presented in Figs. 9 and 10 for the single-ended and differential receiver CBCGs, respectively. In each figure, eye diagrams with noise generation amplitudes of (a) 0 mV and (b) 100 mV are shown. For the single-ended design, only the four best of the eight eye diagrams are shown. Duty-cycle distortion is evident even without switching noise present; when included in the simulations, the eyes are severely degraded. The eye diagrams of the four other receivers were fully closed with switching noise included. These poor operational yield results are consistent with [17]. For the differential design, all of the eye diagrams are exemplary with no switching noise present and remain open when switching noise is included in the simulations.

Additional simulations were performed to demonstrate the versatility of the differential design in the presence of nonuniform $\mathrm{I_{AVG}}$ and $\Delta \mathrm{i_{PH}}$ for the differential preamplifier inputs. For these simulations, the data rate was 250 Mb/s, power supply switching-noise amplitudes of 100 mV were used, and nominal $\mathrm{I_{AVG}}$ and $\Delta \mathrm{i_{PH}}$ values of 55 and 50 μA were used for both preamplifier inputs, respectively. Fig. 11(a) and (b) shows simulated eye diagrams for the cases where $\mathrm{I_{AVG}}$ was reduced by 20% for the (a) inverting and (b) noninverting preamplifier input with respect to the other input, for which $\mathrm{I_{AVG}}$ remained at 55 μA. $\Delta \mathrm{i_{PH}}$ was 50 μA for both inputs. Fig. 11(c) and (d) shows simulated eye diagrams for the cases where the $\Delta \mathrm{i_{PH}}$ was reduced by 20% for the (c) inverting and (d) noninverting preamplifier input with respect to the other input, for which $\Delta \mathrm{i_{PH}} = 50$ μA. $\mathrm{I_{AVG}}$ was 55 μA for both inputs. In all four cases, the receiver remained functional, with only an increase in jitter observed.

V. Conclusion

We have provided an analysis of the design and implementation of large, 2-D arrays of receiver and transmitter circuits for use in OE-VLSI applications. We have described the design environment of an OE-VLSI chip and the strong influence of the digital circuitry on the design and test flow of the receiver and transmitter circuits. There are severe constraints on physical space available for circuit implementation and on the aggregate power dissipation of the receiver and transmitter arrays, which can limit the circuit and application complexity that can be implemented. The influence of the digital circuitry on the design and test flows of the receiver and transmitter provides an opportunity for significant advancement in test methodologies. The lack of tight bounds on the throughput uniformity of large-scale optical systems provides a unique challenge for the implementation of large receiver arrays. We have shown that an optically and electrically differential architecture is optimal in overcoming these design challenges for the implementation of large receiver and transmitter arrays for OE-VLSI applications.

We have detailed the inclusion of DFT features to enable the testing of OE-VLSI receivers and transmitters, as well as the implementation test methodologies compatible with conventional digital test techniques, and the integration of these methodologies at the chip level. We have described the benefits of a fully differential architecture in combating the detrimental effects of switching noise, as well as some design considerations to improve the switching-noise performance of receiver and transmitter circuits. Finally, we have demonstrated that the operational yield of receiver CBCGs is significantly improved when an optically and electrically differential architecture, rather than a single-ended architecture, is employed.

Acknowledgment

The authors would like to acknowledge the contributions of E. Laprise, J. Faucher, J.-P. Thibodeau, J. Schwartz, L. Malic, E. Shoukry, and E. Lugo.

References

[1] M. W. Haney, H. Thienpont, and T. Yoshimura, *IEEE J. Select. Topics Quantum Electron.*, vol. 9, pp. 347–667, Mar./Apr. 2003.

[2] *Proc. IEEE*, vol. 88, Y. Li, E. Towe, and M. W. Haney, Eds., June 2000, pp. 723–878.

[3] N. M. Jokerst, R. Baets, and K. Kobayashi, *IEEE J. Select. Topics Quantum Electron*, vol. 5, pp. 143–398, Mar./Apr. 1999.

[4] A. V. Krishnamoorthy, J. E. Ford, F. E. Kiamilev, R. G. Rozier, S. Hunsche, K. W. Goossen, B. Tseng, J. A. Walker, J. E. Cunningham, W. Y. Jan, and M. C. Nuss, "The AMOEBA switch: An optoelectronic switch for multiprocessor networking using dense-WDM," *IEEE J. Select. Topics Quantum Electron.*, vol. 5, pp. 261–275, Mar./Apr. 1999.

[5] A. L. Lentine, K. W. Goossen, J. A. Walker, L. M. F. Chirovsky, L. A. D'Asaro, S. P. Hui, B. J. Tseng, R. E. Leibenguth, J. E. Cunningham, W. Y. Jan, J.-M. Kuo, D. W. Dahringer, D. P. Kossives, D. D. Bacon, G. Livescu, R. L. Morrison, R. A. Novotny, and D. B. Buchholz, "High-speed optoelectronic VLSI switching chip with $>$ 4000 optical I/O based on flip-chip bonding of MQW modulators and detectors to silicon CMOS," *IEEE J. Select. Topics Quantum Electron.*, vol. 2, pp. 77–84, Apr. 1996.

[6] A. L. Lentine, K. W. Goossen, J. A. Walker, J. E. Cunningham, W. Y. Jan, T. K. Woodward, A. V. Krishnamoorthy, B. J. Tseng, S. P. Hui, R. E. Leibenguth, L. M. F. Chirovsky, R. A. Novotny, D. B. Buchholz, and R. L. Morrison, "Optoelectronic VLSI switching chip with greater than 1 Tbit/s potential optical I/O bandwidth," *Electron. Lett.*, vol. 33, pp. 894–895, May 1997.

[7] A. C. Walker, M. P. Y. Desmulliez, M. G. Forbes, S. J. Fancey, G. S. Buller, M. R. Taghizadeh, J. A. B. Dines, C. R. Stanley, G. Pennelli, A. R. Boyd, P. Horan, D. Byrne, J. Hegarty, S. Eitel, H.-P. Gauggel, K. H. Gulden, A. Gauthier, P. Benabes, J.-L. Gutzwiller, and M. Goetz, "Design and construction of an optoelectronic crossbar switch containing a terabit per second free-space optical interconnect," *IEEE J. Select. Topics Quantum Electron.*, vol. 5, pp. 236–249, Mar./Apr. 1999.

[8] M. B. Venditti, E. Laprise, J. Faucher, P.-O. Laprise, J. E. Lugo, and D. V. Plant, "Design, test, and verification of an optoelectronic-VLSI chip with 540-element receiver/transmitter arrays using differential optical signaling," *IEEE J. Select. Topics Quantum Electron.*, vol. 9, pp. 361–379, Mar./Apr. 2003.

[9] R. G. Rozier, F. E. Kiamilev, and A. V. Krishnamoorthy, "Design and evaluation of a photonic FFT processor," *J. Parallel Distrib. Comput.*, vol. 41, pp. 131–136, 1997.

[10] C. B. Kuznia, J.-M. Wu, C.-H. Chen, B. Hoanca, L. Cheng, A. G. Weber, and A. A. Sawchuk, "Two-dimensional parallel pipeline smart pixel array cellular logic (SPARCL) processors—Chip design and system implementation," *IEEE J. Select. Topics Quantum Electron.*, vol. 5, pp. 376–386, Mar./Apr. 1999.

[11] N. McArdle, M. Naruse, and M. Ishikawa, "Optoelectronic parallel computing using optically interconnected pipelined processing arrays," *IEEE J. Select. Topics Quantum Electron.*, vol. 5, pp. 250–260, Mar./Apr. 1999.

[12] C.-S Li, H. S. Stone, Y. Kwark, and C. M. Olsen, "Fully differential optical interconnections for high-speed digital systems," *IEEE Trans. VLSI Syst.*, vol. 1, pp. 151–163, June 1993.

[13] C.-S Li and H. S. Stone, "Differential board/backplane optical interconnects for high-speed digital systems Part I: Theory," *J. Lightwave Technol.*, vol. 11, pp. 1234–1249, July 1993.

[14] C. M. Olsen and C.-S Li, "Differential board/backplane optical interconnects for high-speed digital systems Part II: Simulation results," *J. Lightwave Technol.*, vol. 11, pp. 1250–1262, July 1993.

[15] A. G. Kirk, D. V. Plant, T. H. Szymanski, Z. G. Vranesic, F. A. P. Tooley, D. R. Rolston, M. H. Ayliffe, F. K. Lacroix, B. Robertson, E. Bernier, and D. F.- Brosseau, "Design and implementation of a modulator-based free-space optical backplane for multiprocessor applications," *Appl. Opt.*, vol. 42, pp. 2465–2481, May 2003.

[16] D. R. Rolston, D. V. Plant, T. H. Szymanski, H. S. Hinton, W. S. Hsiao, M. H. Ayliffe, D. Kabal, M. B. Venditti, A. V. Krishnamoorthy, K. W. Goossen, J. A. Walker, B. Tseng, S. P. Hui, J. C. Cunningham, and W. Y. Jan, "A hybrid-SEED smart pixel array for a four-stage intelligent optical backplane dem-onstrator," *IEEE J. Select. Topics Quantum Electron.*, vol. 2, pp. 97–105, Apr. 1996.

[17] D. V. Plant, M. B. Venditti, E. Laprise, J. Faucher, K. Razavi, M. Chateauneuf, A. G. Kirk, and J. S. Ahearn, "256 channel bi-directional optical interconnect using VCSEL's and photodiodes on CMOS," *J. Lightwave Technol.*, vol. 19, pp. 1093–1103, Aug. 2001.

[18] E. Säckinger and W. Fischer, "A 3-GHz 32-dB CMOS limiting amplifier for SONET OC-48 receivers," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1884–1888, Dec. 2000.

[19] W.-Z. Chen and C.-H. Lu, "A 2.5 Gbps CMOS optical receiver analog front-end," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2002, Paper 20–2, pp. 359–362.

[20] H. Ikeda, T. Ohshima, M. Tsunotani, T. Ichioka, and T. Kimura, "An auto-gain control transimpedance amplifier with low noise and wide input dynamic range for 10-Gb/s optical communications systems," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1303–1308, Sept. 2001.

[21] R. M. Hickling, R. A. Kot, M. N. Yagi, R. Nagarajan, W. J. Sha, and R. Craig, "Low power components for 1 Gb/s optical communications: A single-chip 10-channel optical receiver and a clock recovery circuit," in *Proc. Gallium Arsenide Integrated Circuit Symp.*, 1997, pp. 201–204.

[22] T. K. Woodward, A. V. Krishnamoorthy, A. L. Lentine, and L. M. F. Chirovsky, "Optical receivers for optoelectronic VLSI," *IEEE J. Select. Topics Quantum Electron.*, vol. 2, pp. 106–116, Apr. 1996.

[23] T. K. Woodward, A. V. Krishnamoorthy, K. W. Goossen, J. A. Walker, J. E. Cunningham, W. Y. Jan, L. M. F. Chirovsky, S. P. Hui, B. Tseng, D. Kossives, D. Dahringer, D. Bacon, and R. E. Leibenguth, "Clock-sense-amplifier-based smart-pixel optical receivers," *IEEE Photon. Technol. Lett.*, vol. 8, pp. 1067–1069, Aug. 1996.

[24] M. Châteauneuf, A. G. Kirk, D. V. Plant, T. Yamamoto, and J. D. Ahearn, "512-channel vertical-cavity surface-emitting laser based free-space optical link," *Appl. Opt.*, vol. 41, pp. 5552–5561, Sept. 2002.

[25] T. Maj, A. G. Kirk, D. V. Plant, J. F. Fonstad, K. L. Lear, K. Tatah, M. S. Robinson, and J. A. Trezza, "Interconnection of a two-dimensional array of vetical cavity surface emitting lasers to a receiver array via a fiber image guide," *Appl. Opt.*, vol. 39, pp. 683–689, Feb. 2000.

[26] T. W. Williams, Ed., *VLSI Testing*. Amsterdam/New York: North-Holland, 1986.

[27] P. H. Bardell, W. H. McAnney, and J. Savir, *Built-in Test for VLSI: Pseudorandom Techniques*, NY: Wiley, 1987.

[28] K. D. Wagner and T. W. Williams, "Design for testability of analog/digital networks," *IEEE Trans. Ind. Electron.*, vol. 36, pp. 227–230, May 1989.

[29] M. H. Hafed, N. Abaskharoun, and G. W. Roberts, "A 4-GHz effective sample rate integrated test core for analog and mixed-signal circuits," *IEEE J. Solid-State Circuits*, vol. 37, pp. 499–514, Apr. 2002.

[30] F. E. Kiamilev and A. V. Krishnamoorthy, "A high-speed 32-channel CMOS VCSEL driver with built-in self-test and clock generation circuitry," *IEEE. J. Select. Topics Quantum Electron.*, vol. 5, pp. 287–295, Mar./Apr. 1999.

[31] C. F. Hawkins, J. M. Soden, A. W. Righter, and F. J. Ferguson, "Defect classes—An overdue paradigm for CMOS IC testing," in *IEEE Int. Test Conf.*, 1994, Paper 18.3, pp. 413–425.

[32] E. Laprise, "Design and Implementation of Optoelectronic-VLSI Chips for Short Reach Optical Interconnects," M. Eng. thesis, McGill University, Montréal, QC, Canada, 2001.

[33] T. K. Woodward, A. L. Lentine, A. V. Krishnamoorthy, K. W. Goossen, J. A. Walker, J. E. Cunningham, W. Y. Jan, B. Tseng, S. P. Hui, and R. E. Leibenguth, "Parallel operation of 50 element two-dimensional CMOS smart-pixel receiver array," *Electron. Lett.*, vol. 34, pp. 936–937, May 1998.

[34] A. V. Krishnamoorthy, R. G. Rozier, T. K. Woodward, P. Chandramani, K. W. Goossen, B. Tseng, J. A. Walker, J. A. Walker, W. Y. Jan, and J. E. Cunningham, "Triggered receivers for optoelectronic-VLSI," *Electron. Lett.*, vol. 36, pp. 249–250, Feb. 2000.

[35] K. R. Shastri, K. N. Wong, and K. A. Yanushefski, "1.7 Gb/s NMOS laser driver," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1988, pp. 5.1.1–5.1.4.

[36] T. K. Woodward and A. V. Krishnamoorthy, "1 Gbit/s CMOS photoreceiver with integrated detector operating at 850 nm," *Electron. Lett.*, vol. 34, no. 12, pp. 1252–1253, June 1998.

Michael B. Venditti (S'94–A'96–M'03) received the B.Eng. (honors), M.Eng., and Ph.D. degrees in electrical and computer engineering from McGill University, Montreal, QC, Canada, in 1996, 1999, and 2003, respectively. His graduate work focused on the design of optical receivers and transmitters, and application-specific integrated circuits (ASICs) design for optoelectronic-very large scale integration (VLSI) applications.

In 1997 and 1999, he was involved in four-month internships at Nortel Networks and Sanders, a Lockheed Martin company (now BAE Systems/TeraConnect Inc.), respectively. In 2000, he was a Faculty Lecturer for the Department of Electrical and Computer Engineering at McGill University. He is now a mixed-signal design engineer at PMC-Sierra, Montreal, QC, Canada. His research interests include optoelectronic devices, free-space optical interconnects, mixed-signal ASIC design, and applications of optoelectronic-VLSI technology.

Dr. Venditti is a Member of the IEEE Lasers and Electro-Optics Society (LEOS), the Solid-State Circuits Society, and the Circuits and Systems Society. He has received undergraduate and graduate scholarships from the Natural Sciences and Engineering Research Council of Canada and from Le Fonds pour la Formation de Chercheurs et l'Aide à la Recherche du Québec. He was awarded a LEOS Graduate Student Fellowship in 2002.

David V. Plant (S'86–M'89) received the Ph.D. degree in electrical engineering from Brown University, Providence, RI, in 1989.

From 1989 to 1993, he was a Research Engineer in the Department of Electrical and Computer Engineering at the University of California at Los Angeles (UCLA). In 1993, he joined the Department of Electrical and Computer Engineering, McGill University, Montreal, QC, Canada, as an Assistant Professor and was promoted to Associate Professor with tenure in 1997. During the 2000–2001 academic year, he was on leave from McGill University to become the Director of Optical Integration at Accelight Networks, Pittsburgh, PA. He has been a Project Leader and Major Project Leader in the Canadian Institute for Telecommunications Research (CITR), based at McGill University, and a Project Leader in the Canadian Institute for Photonic Innovation (CIPI), based at Laval University, Quebec City, QC, Canada. Currently, he is the Scientific Director of the Agile All-Photonic Networks (AAPN) research program of the National Sciences and Engineering Council (NSERC) of Canada, based at McGill University.

Dr. Plant received the Outstanding Departmental Teaching Award and the Faculty of Engineering Teaching Award in 1996. In recognition of his accomplishments in research and teaching, he was named a James McGill Professor in 2001.